Remarks:

Claim Rejections – 35 USC 112

Claim 2 was rejected under the second paragraph of 35 USC 112 as being unclear regarding which p+ and n+ regions are referred to when saying said p+ region is on the high voltage side of said n+ region.

Claim 2 has been amended to define the p-n junction more simply as including one of the additional p+ regions and one of the additional n+ regions. The relative positions of the additional p+ and additional n+ region of the p-n junction is then defined along the wording proposed by the examiner.

Claim Rejections – 35 USC 103

Claims 2-4 were rejected over Ker in view of Yu

a. Regarding claim 2, the Office Action states that Ker teaches a method of increasing the holding voltage of an LVTSCR structure. This is not correct. Ker specifically makes use of a SOI (silicon over insulator) process to address the holding voltage problem that is otherwise found in SCRs. See Description of the Related Art in Ker, column 1, lines 21-24. Ker instead is providing a different type of SCR structure in which the triggering voltage is reduced (see Description of the Related Art in Ker, column 1, lines 15-59 discussing the problem that Ker is seeking to address)

b. The Office Action goes on to state that Ker teaches in figure 8B a method of forming an LVTSCR structure that further comprises forming at least one additional p+ region 222 and at least one n+ region 220 inside the p-well of the structure to define at least one p-n junction …the p+ region of the p-n junction located on the high voltage side …the defined p-n junction. This is also not correct since n+ region 220 is part of the cathode of the LVTSCR as shown in Figure 8A which shows n+ 220 and p+ 218 connected to define the cathode. This is also specifically described in column 9, lines 64-67 of Ker. Thus Figures 8A and 8B of Ker show the cathode and anode but do not show an additional n+ region in the p-well.

Regarding claims 3-4, the same arguments are made in the Office Action about Ker teaching a method of increasing the holding voltage of an LVTSCR and forming at least one

additional p+ region 222 and at least one n+ region 220 inside the p-well. As discussed above, Ker does not teach either of these two aspects.

The Office Action goes on to state that Ker does not teach in Figure 8B an n+ region and a p+ region. As discussed above, Ker does in fact deal with an LVTSCR that has an n+ region 220 and a p+ region 218 connected to define the cathode as described in column 9, lines 64-67 of Ker.

The Office Action goes on to state that Ker teaches in Figure 10B a diode 324 connected to the cathode. This is correct. In fact it clearly shows Ker contemplating the use of an external diode series – see also the discussion at column 11, lines 33-35. It is specifically this inclusion of external diodes that the present invention seeks to avoid as is clear from the discussion in the acknowledged prior art in its Background section at page 7, lines 6-13. The present invention seeks to provide a solution to the inherent problems involved in such an external diode string. This further shows that Ker teaches only external diodes and does not suggest integrated diodes in the LVTSCR structure.

The Office action then points to Yu as teaching a diode formed in a p-substrate. Applicant does not deny that diodes formed in a p-substrate exist in the prior art. In fact Ker itself discloses in Figure 8A a p-substrate with p+ and n+ regions. In fact, as early as 1998, in patent 5,754,380 the same inventor Ker taught a p-substrate with p+ region and n+ region. Thus, in spite of being aware of the existence of diodes in a p-substrate, it did not suggest to Ker to create an integrated set of diodes in an LVTSCR structure as proposed by the present invention to address the latch-up problem. As mentioned above, Ker instead addresses latch-up by making use of a SOI process. In the same way, any other person skilled in the art, faced with the problem of latch-up in LVTSCRs and having Ker at his disposal, would recognize that the SOI process used by Ker already addresses the latch-up problem, thereby not requiring additional diodes to address latch-up.

It is therefore not surprising that there is no teaching or even a suggestion in either of the cited references to include integrated diodes to avoid the latch-up problem of an LVTSCR. Therefore it cannot be said to be obvious to combine the two cited references to achieve the benefits discussed by the present application at page 9, line 23 to page 10, line 12, namely: *"It provides for a simple interconnect layout and a compact design by providing a straightforward serial arrangement. Simulation results have also shown that compared to prior art high holding*

voltage SCR designs, the present invention displays little sensitivity to process variations, doping levels, and dimension variations. Figure 8 shows voltage curves 800, 802, and 804 for widths w=25μm, 50μm, and 100μm, respectively. Furthermore, since the diodes are formed inside the grounded p-well 402, the structure does not increase the capacitance over that of a conventional LVTSCR. This is illustrated by the curves in Figure 9 showing the capacitance variation with drain-source bias for a conventional device (curve 900) compared to that of a device of the invention (curve 902). Figure 9 also shows that the conductance curves for a device of the invention (curve 904) remains essentially the same as that for a conventional LVTSCR (curve 906). Furthermore, the holding voltage displays a low temperature curve. Referring to Figure 10, the lattice temperature variation for a device of the invention (curve 1000) is substantially the same as that for a conventional device (curve 1002). Also, the holding voltage is shown to be higher for the device of the invention." (underlining was added for emphasis)

There is nothing in the cited references that suggests that they were aware of the above benefits. The only issue above that is addressed by Ker is the high holding voltage in order to reduce latch-up, which Ker addresses in an entirely different way, by making use of a SOI process.

Response to Arguments

The Office Action states that Ker teaches a diode in forward bias during normal operation. As stated above, it cannot therefore be obvious to a person skilled in the art to look either at Ker itself or Yu together with Ker to come up with the present invention, since Ker (as a person skilled in the art himself) instead chose to use external diodes and a SOI process to achieve its purposes.

Respectfully Submitted,

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